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The application is published incomplete as filed (Article 93 (2) EPC). The point in the description at which the omission obviously occurs has been left blank.(Pages 7 and 8 of the originally filed description are missing)

A request for addition of pages of the description has been filed pursuant to Rule 88 EPC. A decision on the request will be taken during the proceedings before the Examining Division (Guidelines for Examination in the EPO, A-V, 2.2).

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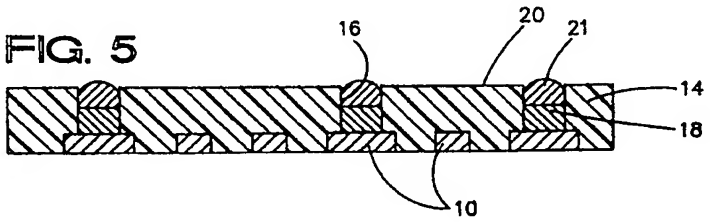
## (54) Method of manufacturing a multilayer circuit board.

(57) Methods of fabricating multilayer circuits are presented. In accordance with the present invention, a plurality of circuit layers comprised of a dielectric substrate having a circuit formed thereon are stacked, one on top of the other. The dielectric substrate is composed of a polymeric material capable of undergoing fusion bonding such as a fluoropolymeric based substrate. Fusible conductive bonding material (e.g. solder) is applied in selected exposed circuit traces (prior to the stacking step) whereupon the entire stack-up is subjected to lamination under heat and pressure to simultaneously fuse all of the substrate and conductive layers together to form an integral multilayer circuit having solid conductive interconnects.

FIG. 5

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This invention relates generally to methods of manufacturing multilayer circuit board and multichip modules. More particularly, this invention relates to new and improved methods of manufacturing multilayer circuits wherein interconnections between circuit layers may be accomplished in a single fusion bonding lamination step utilizing fusible conductive material. In a preferred embodiment, this fusion bonding is accomplished without the need for intermediate bonding plys.

Multilayer circuits are well known and comprise a plurality of stacked substrate/circuit trace assemblies with interconnections between selected locations on the spaced circuit traces. These circuits are often configured as stripline or microstrip circuits and find particular utility in microwave antenna and other microwave applications. These circuits are also used in the manufacture of multichip modules. Conventional manufacturing techniques for multilayer circuits sometimes require multiple bonding cycles to make the completed assembly. Once the substrates have been bonded together, via holes are drilled completely through the bonded assembly and plated for transferring electrical connections between different layers. This limits the circuit density and the number of substrates. The bonding material, which may comprise a bonding film between the substrates, tends to flow out of the assembly under the influence of the high temperature and pressure. As more and more of the bonding material flows out, the pressure is tranferred to the plated holes which may collapse and/or be pushed into the substrate which has been softened by the high temperature.

U.S. Patent N° 4,788,766 attempts to overcome these problems. This prior patent discloses a method wherein a multilayer assembly is made up of a number of individual circuit boards and each board has a substrate on which a first conductive layer is formed on the opposite surface. The substrate is a dielectric material which insulates the conductive layers. Via holes are formed through the first conductive layer, the substrate and the second conductive layer at various locations. An outer conductive material, such as copper, is applied over the first and second conductive bonding layers and onto the side walls of the holes. A conductive bonding material is then deposited onto the outer conductive material in the areas around the holes. Once the individual boards have been fabricated, they are stacked in a predetermined order and orientation with a suitable low temperature dielectric bonding ply (meaning that the bonding ply has a lower softening temperature than the circuit substrate material) positioned between each pair of layers. The dielectric bonding ply requires registered apertures therethrough which correspond to areas where the conductive layer of one substrate is to make an electrically conductive connection with the conductive layer of an adjacent substrate. Thus, the dielectric bonding ply integrally bonds adjacent boards together while providing electrical isolation and/or electrical connections between conductive layers of the different boards. The assembly of boards is then subjected to a cycle of heat and pressure to effect a bond between the various board layers.

While the method of U.S. Patent 4,788,766 overcomes some of the problems in the prior art, this prior method has certain disadvantages including the requirement for a substrate which has a melting temperature above the melting temperature of the bonding ply. In other words, the prior patent necessitates the use of a low temperature bond ply which limits the thermal rating of the multi-layer circuit. In addition, this prior method necessitates registered apertures in the bonding ply (leading to alignment problems) and is limited to multilayer circuits having plated through holes.

The purpose of the present invention is to overcome or alleviate the above-discussed and other problems and deficiencies of the prior by the methods of fabricating multilayer circuits of the present invention.

In accordance with the present invention, a plurality of circuit layers comprised of a dielectric substrate having a circuit formed thereon are stacked, one on top of the other. The dielectric substrate is composed of a polymeric material capable of undergoing fusion bonding such as a fluoropolymeric based substrate. Fusible conductive bonding material (e.g. solder) is applied on selected exposed circuit traces (prior to the stacking step) whereupon the entire stack-up is subjected to lamination under heat and pressure to simultaneously fuse all of the substrate and conductive layers together to form an integral multilayer circuit having solid conductive interconnects.

In a first embodiment of the present invention, the discrete circuit layers are each prepared by (1) forming traces and pads on a removable mandrel; (2) laminating a layer of dielectric to the circuit and mandrel; (3) forming an access opening at selected locations through the dielectric layer (using laser, plasma, ion etch or mechanical drilling techniques) to expose selected circuit locations; (4) forming conductive posts in the access openings to a level below the top of the access openings; and (5) providing a fusible conductive material in the access opening. Therafter, a stack-up is made of a plurality of these discrete circuit layers so that the exposed fusible conductive material contacts selected locations on an adjacent circuit. This stack-up is then subjected to heat and pressure to simultaneously fuse both the several layers of dielectric substrate and fusible conductive material to provide a cohesive fused multilayer

circuit board.

In a second embodiment of this invention, at least one discrete circuit board is made using any suitable technique to define a fusible dielectric substrate having a circuit pattern thereon. Next, a layer of fusible dielectric material having openings through selected locations is placed on the circuit board so that selected locations on the circuit pattern are exposed. Thereafter, a plug of fusible conductive material (e.g. solder) is placed in the openings (using manual, mechanical or like techniques). Next, a second circuit board is stacked on the first board so that the plugs of fusible conductive material align with and contact selected locations on the circuit pattern in the second circuit board. This stack-up is then subjected to heat and pressure to simultaneously fuse both the layers of fusible dielectric and the fusible conductive material to provide a cohesive fused multilayer circuit board.

All of the foregoing embodiments provide important features and advantages relative to prior art multilayer circuit fabrication techniques including lower manufacturing costs and increased circuit density.

The above-discussed and other features and advantages of the present invention will be appreciated and understood by those skilled in the art from the following detailed description and drawings.

Referring now to the drawings, wherein like elements are numbered alike in the several FIGURES :

FIGURES 1-5 are sequential cross-sectional elevational views showing the fabrication of a discrete circuit board layer in accordance with the first embodiment of the present invention;

FIGURE 6 is an exploded view depicting a stack-up of circuit boards of the type shown in FIGURE 5;

FIGURE 7 is a cross sectional elevation view of a final laminated multilayer circuit board made in accordance with the first embodiment of the present invention; and

FIGURES 8-12 are cross sectional elevation views depicting a sequential fabrication technique for making multilayer circuit boards in accordance with the second embodiment of the present invention.

The present invention relates generally to methods of interconnecting individual layers of a multichip module or multilayer circuit board using fused polymer composite bonding. All of the inner layers of the circuit boards are interconnected using fusible metal posts or the like to achieve solid constructive interconnects. These fusible posts can be composed entirely of fusible conductive material or a combination of non-fusible and fusible conductive materials. The fusible conductive material may be introduced into the mutilayer circuits using any number of techniques which will be described below. In addition, the present invention generally utilizes a fusible dielectric substrate which fuses with adjacent layers of dielectric substrate concurrently with the fusible conductive metal.

Examples of suitable fusible dielectric substrates include fluoropolymer based substrate materials such as PTFE or the fluoropolymeric susbtrates described in U.S. Patent Nos 4,335,180; 4,634,631; 4,647,508 or 4,849,284. Examples of commercially available dielectric substrates suitable for the present invention include the materials sold under the tradenames RT/DUROID and RO-2800, both of which are available from Rogers Corporation, assignee of the present application. Examples of suitable fusible conductive material include metals and metal alloys with a melting point of less than 482 $^{\circ}$C. A specific example of such a fusible material is a solder composition of 60 % tin and 40 % lead.

Turning now to FIGURES 1-7, a first embodiment of the present invention will now be described . In the first step shown in FIGURE 1, a pattern of 10 of circuit traces and pads is formed on suitable mandrel 12. The pattern may be comprised of any suitable conductive material such as copper or aluminum and may be formed on mandrel 12 by any suitable method such as electroless plating, electroplating or vapor deposition. Mandrel 12 is preferably comprised of copper or other metal. Next, as shown in FIGURE 2, a layer of dielectric material 14 is laminated over circuit 10 and mandrel 12. Thereafter, access openings 16 are provided through dielectric layer 14 at selected locations to access the pads or traces 10 (see FIGURE 3).

Access openings 16 may be formed using any known means such as laser, plasma, ion etch or mechanical drilling techniques. One particularly well suited technique is the laser etching methodology described in EP application 0380634.

After the access openings 16 has been formed (see FIGURE 4), conductive posts 18 are formed within access openings 16 so as to completely fill openings 16 to a level just below the top surface 20 of dielectric layer 14. Still referring to FIGURE 4, in the next step, a conductive fusible material such as solder is disposed in the remaining portion of access opening 16 so as either to be level with top surface 20 or extend slightly thereover. In the final step of forming a discrete circuit layer, the mandrel 12 is removed from the circuit and dielectric using any suitable removal methods such as known etching techniques. The final discrete circuit layer is thus shown at 22 in FIGURE 5.

Turning now to FIGURE 6, a plurality of circuits 22 which have been fabricated in accordance with the techniques shown in FIGURES 1-5 are stacked one on top of the other in the manner shown. Of course, any number ($X_n$) of circuit substrates 22 may be stacked and registered with one another such that the fusible

conductive material 21 aligns with a selective location on an adjacent circuit pad or trace 10.

Example 2 :

A circuit laminate with circuit features substractively defined was prepared as in FIGURE 8. The fusible substrate was the material described in U.S. Patent 4,849,284 and sold commercially under the trademark

RO-2800 by Rogers Corporation. Next, a layer of bonding ply with apertures defined in the areas where fusible interconnects were to be formed was registered to these circuit features and layed up as in FIGURE 9. The bonding ply was the material sold by Rogers Corporation under the trademark RO-2810. Solder plugs (approximately 3,2 mm in diameter) having a 3 % tin, 97 % lead composition were then placed in the apertures as in FIGURE 10. Another circuit laminate was then registered to the tooled bond ply and layed up as shown in FIGURE 11. The stack-up was then laminated at 390 °C and $17{,}2.10^5$ PA for one hour with the dielectric and solder materials separately fusing to form a cohesive multilayer interconnect structure. The circuit material in both Examples 1 and 2 were copper.

In general, the fusion bonding will take place in a temperature range of between the melting point of the fusible dielectric and the degradation temperature of the fusible dielectric. When using a PTFE fluoropolymer based substrate, this temperature range will be between 325 °C and 425 °C. A preferred pressure range is between $17{,}2.10^5$ to $117.10^5$ PA.

This invention presents unexpected and surprising results in that while the dielectric fuses and therefore undergoes a degree of flow, the flow is insubstantial and will not adversely effect circuit layer orientation and layer-to-layer alignment. Thus, precision multi-layer circuit may be made from the method of this invention.

## Claims

1. A method of making a multilayer circuit comprising the steps of :
   providing at least two circuit boards wherein said first circuit board comprises a first substrate of fusible dielectric material and a first conductive circuit formed thereon and said second circuit board comprises a second substrate of fusible dielectric material and a second conductive circuit formed thereon and wherein at least said first conductive circuit includes fusible conductive material provided on at least one selected location thereof;
   stacking said at least two circuit boards one on top of the other so that said fusible conductive material on said first circuit aligns with a selected location on said second circuit;
   laminating said stacked circuit boards under heat and pressure effective to fuse both said fusible dielectric material and said fusible conductive material so as to form a cohesive multilayer circuit having a solid conductive interconnect between said first and second circuits, said solid conductive interconnect being defined by said fusible conductive material.

2. A method in accordance with claim 1 wherein at least one of said two circuit boards are formed using the steps of :
   forming a circuit pattern;
   forming a fusible dielectric substrate having opposed first and second surfaces, said circuit pattern being located on said first surface of said substrate;
   forming at least one access opening through said second surface of said substrate to expose a selected location in said circuit pattern;
   filling said access opening with conductive material wherein at least an upper portion of said filled access opening comprises fusible material.

3. A method in accordance with claim 2 wherein :
   a lower portion of said access opening comprises non-fusible conductive material.

4. A method in accordance with claim 2 including the step of :
   forming said circuit pattern on a mandrel prior to forming said dielectric substrate on said circuit pattern.

5. A method in accordance with claim 4 including the step of :
   removing the mandrel subsequent to filling the access opening with conductive material.

6. A method in accordance with claim 1 including the step of :
   forming said fusible conductive material as a plug in a sheet of fusible dielectric material which is sandwiched between said two circuit boards.

7. A method in accordance with claim 1 wherein :
   said access opening is formed by at least one of the opening formation techniques selected from

the group consisting of laser drilling, mechanical drilling, plasma etching and ion etching.

8. A method in accordance with claim 1 wherein :
said fusible dielectric material comprises a fluoropolymeric material.

9. A method in accordance with claim 8 wherein :
said fluoropolymeric material comprises a polytetrafluoroethylene based material.

10. A method in accordance with claim 1 wherein :
said fusible conductive material comprises a metal or metal alloy.

11. A method in accordance with claim 10 wherein :
said fusible conductive material has a melting point of less than 482 °C;

12. A method in accordance with claim 1 wherein said heat is in the temperature range of 325 °C to 425 °C.

FIG. 1

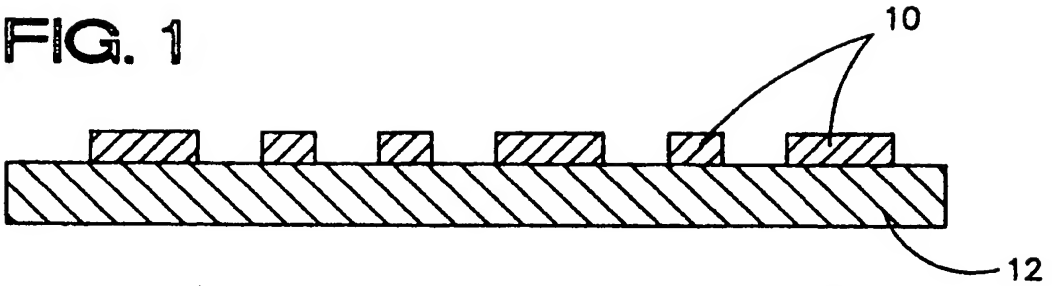



FIG. 2

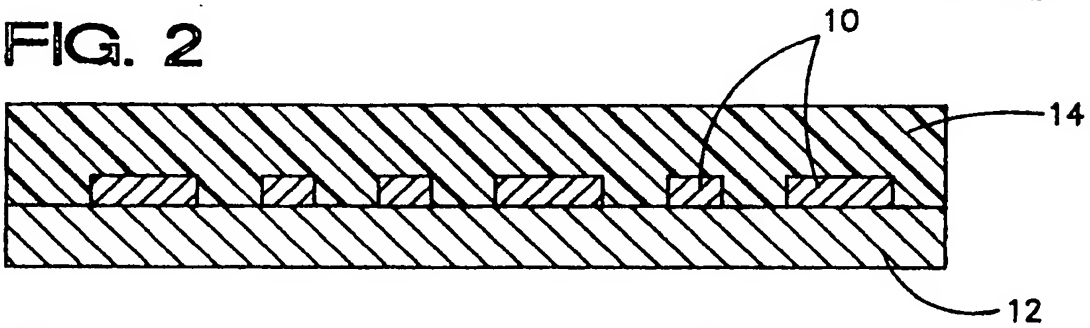



FIG. 3

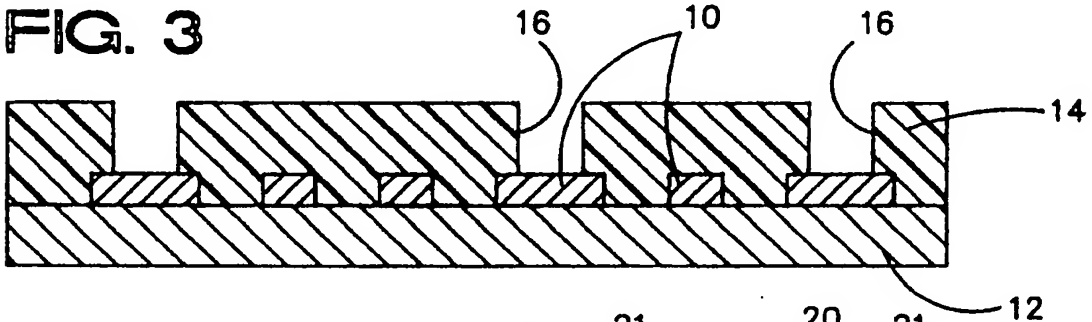



FIG. 4

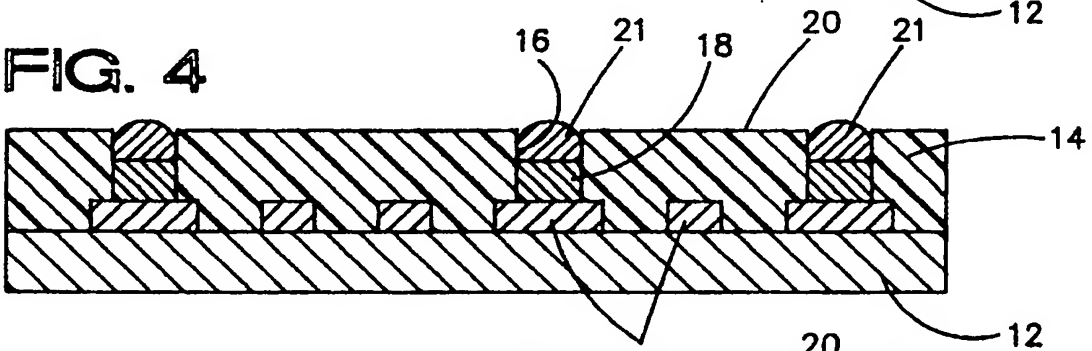



FIG. 5

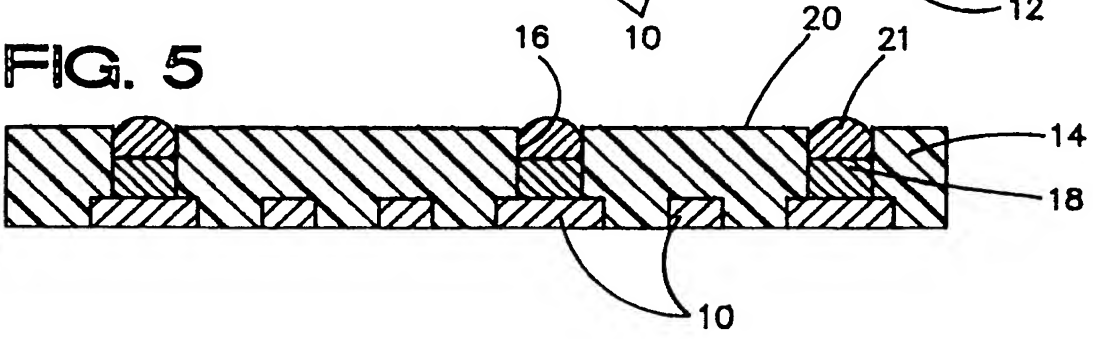


FIG. 6

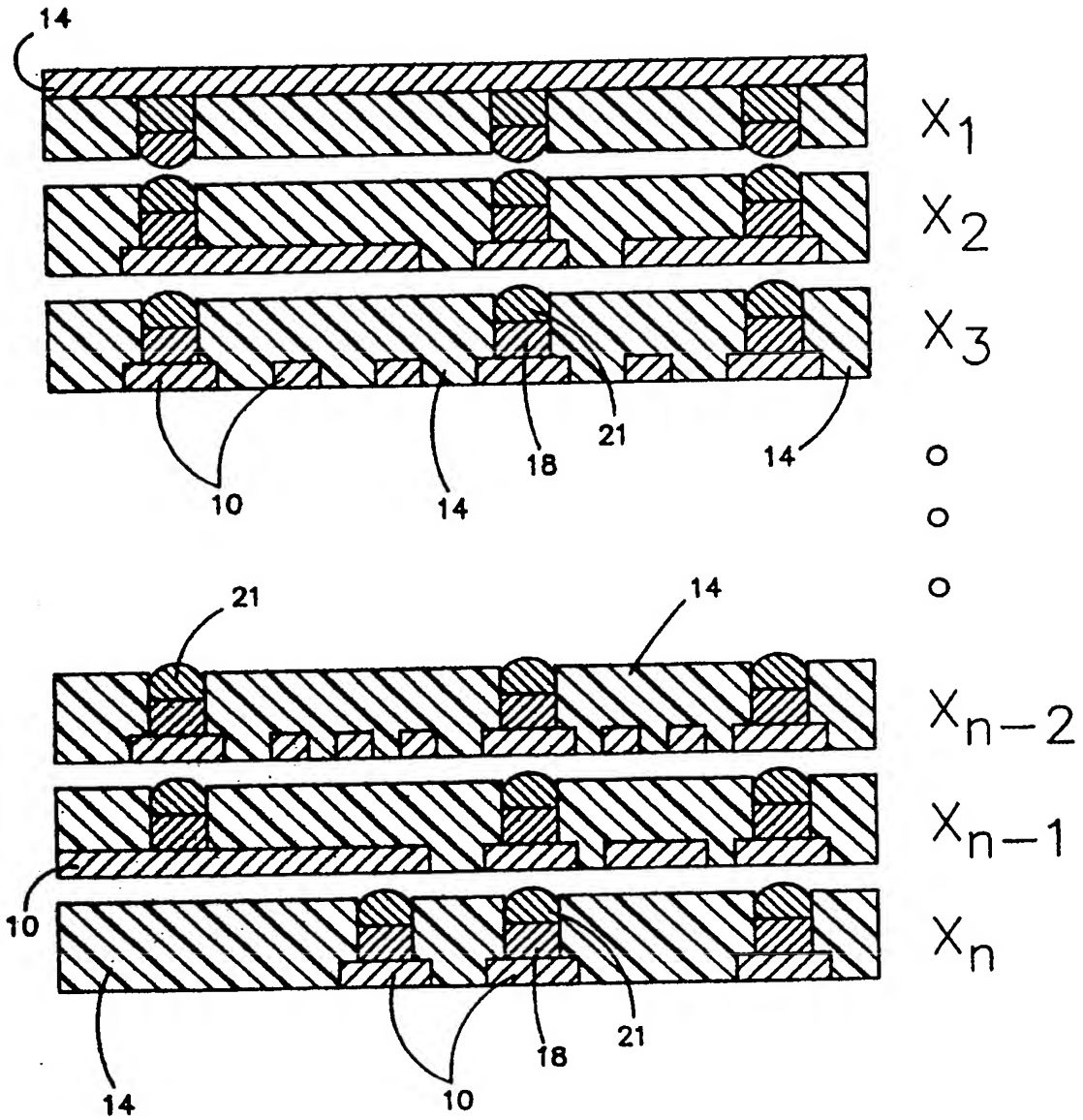


FIG. 7

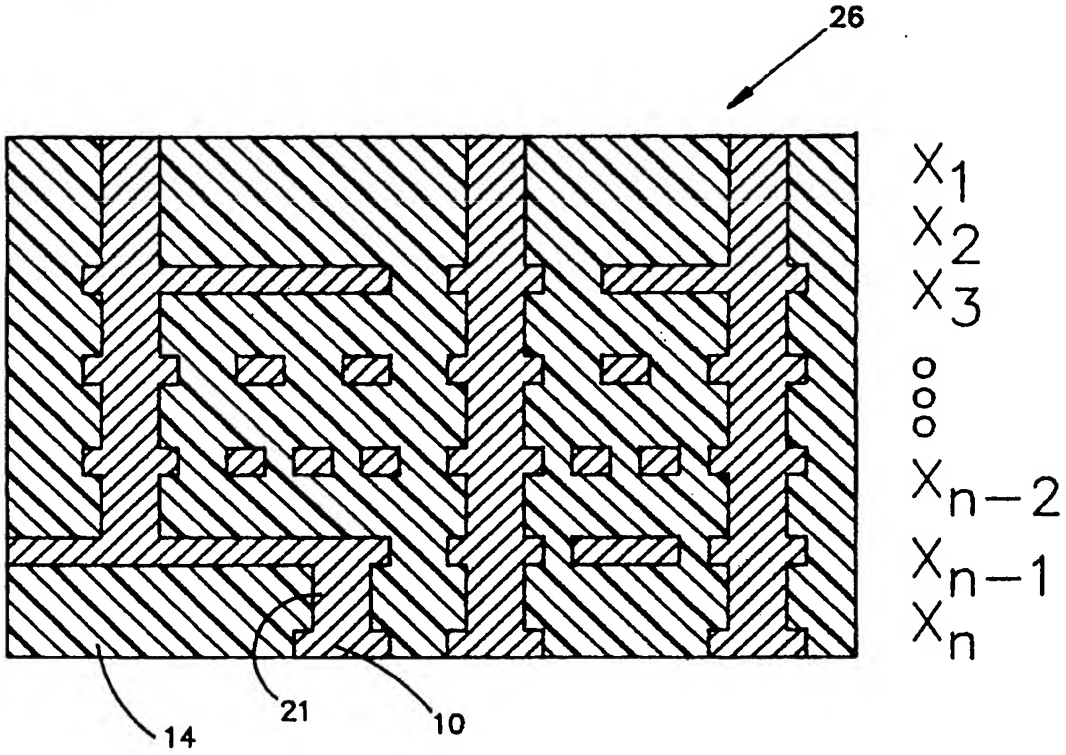


FIG. 8

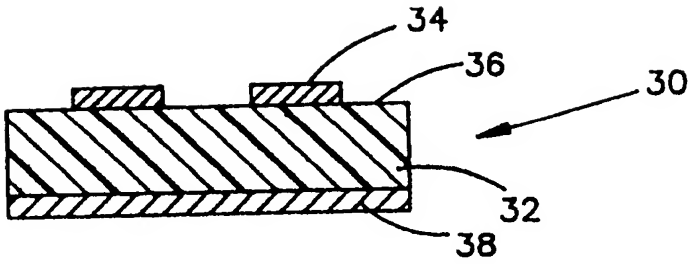



FIG. 9

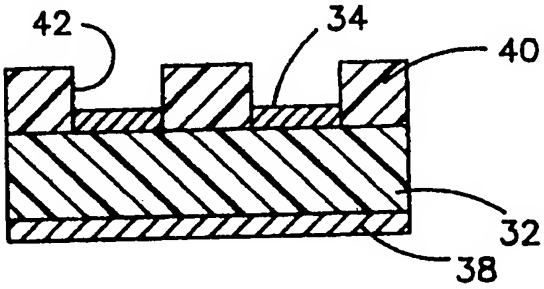



FIG. 10

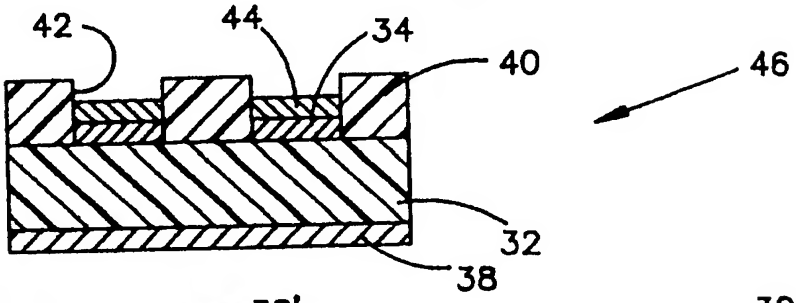



FIG. 11

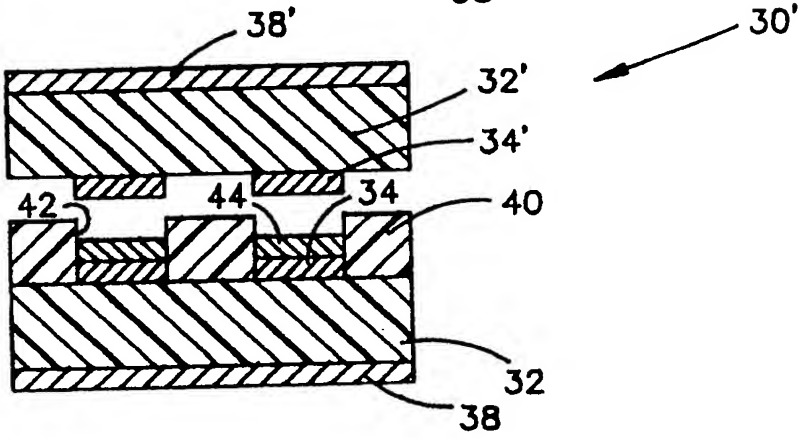
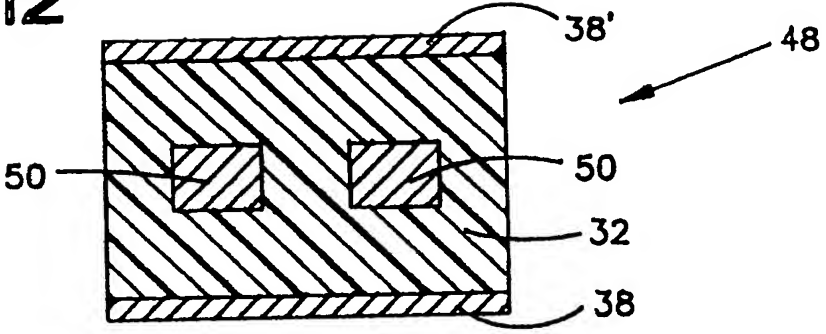



FIG. 12



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# EUROPEAN SEARCH REPORT

Application Number

## DOCUMENTS CONSIDERED TO BE RELEVANT

EP 91102311.7

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| A | EP - A2 - 0 232 026 (IMPERIAL CHEMICAL IND.) * Abstract; fig. 1-7; claims 1-10 * | 1-12 | H 05 K 3/46 |
| A | EP - A1 - 0 275 686 (PRESTWICK CIRCUITS LTD.) * Abstract; fig. 2,3; claims 1-10 * | 1-12 | |
| P,A | EP - A1 - 0 374 272 (E.I. DU PONT) * Abstract; fig. 1,2; claims 1-7 * | 1-12 | |
| A | DE - A1 - 3 541 977 (ROTH) * Abstract; fig. 1-3; claims 1-4 * | 1-12 | |
| A | DE - A1 - 3 639 443 (ANT NACHRICHTENRECHNIK) * Abstract; fig. 1-6; claims 6-8 * | 1-12 | TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 05 K 3/00 |
| D,A | US - A - 4 849 284 (ARTHUR) * Abstract; fig. 1-3 * | 1-12 | |
| D,A | US - A - 4 788 766 (BURGER) * Abstract; fig. 1-4 * | 1-12 | |
| D,A | US - A - 4 647 508 (GAZIT) * Abstract; fig. 1-7 * | 1-12 | |
| D,A | US - A - 4 335 180 (TRAUT) * Abstract; claims 1-14 * | 1-12 | |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| VIENNA | 17-06-1991 | VAKIL |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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|---|---|---|---|
| D,A | US - A - 4 634 631 (GAZIT) * Abstract; fig. 1-9 * | 1-12 | |

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

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